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EXAMINER	
RADOSEVICH, STEVEN D	

ART UNIT	PAPER NUMBER
2138	

DATE MAILED: 11/13/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/637,663	ITOH ET AL.	
	Examiner	Art Unit	
	Steven D. Radosevich	2138	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *14 August 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-16* is/are rejected.

7)☒ Claim(s) *1,8 and 12* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *11 August 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *7/20/06*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claims 1-16 are present for this continued examination of the instant application.

Priority

Acknowledgement is made that foreign priority is claimed for this application and as such the date 02/13/2003 is being used for this continued examination of the instant application.

Information Disclosure Statement

Acknowledgement is made that an Information Disclosure Statement (IDS) was provided with the instant application upon filing with the office prior to the point of this examination but after the final examination of the application mailed to applicant on 05/12/2006. At this time of continued examination of the instant application this IDS filed and submitted to the office on 07/20/2006 has been fully considered and reviewed.

Drawings

Figure 10 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the

applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

Claims 1 and 8 are objected to because of the following informalities:

There is an improper spacing after "test signal," and "the assembly comprising:" within lines 3-4 within the claims.

Appropriate correction is required.

Claim 5 is objected to because of the following informalities:

There is an identical issue within lines 2-3 of the claim as described above in claims 1 and 8 after "the target LSI, and" within the claim.

Appropriate correction is required.

Claim 12 is objected to because of the following informalities:

There is an improper punctuation at the end of line 5 of the claim as is appears within the application, the "," should be replaced with a ":" to indicate a listing of the limitation within the assembly is to follow, which is what is believe to be the case.

Further there is again an improper spacing after "test signal," and "wherein the assembly comprising," within lines 4-5 within the claim.

Additionally there is improper indentation within the limitations following what is comprised within the assembly, the three limitation listed and believed to be within the assembly should be further indented to indicate they are present

within the assembly, which is the second limitation within the test system. As it appears the three limitations are not within the assembly but within the test system.

Appropriate correction is required

Response to Arguments

Applicant's arguments with respect to claim 1-16 have been considered but are moot in view of the new ground(s) of rejection.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 13 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 13, it is unclear to the examiner if the "reference test result signal" within the last limitation within the claim in last line of the claim is the same or different from the "reference test result signal" previously introduced within line 4 of the claim. Appropriate correction and or explanation is required. Examiner suggests inserting "the" or "said" directly prior to the "reference test result signal" in the last time of the claim is applicant desires to indicate that it is the same "reference test result signal" as indicated within line 4 of the claim. For the purposes of this examination the "reference test result

signal" will be treated as either the same or different from the "references test result signal" as introduced within line 4 of the claim.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 1, 12, 14, and 16 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) as described within the instant application's description of the related art within the background of the invention and/or within the U.S. Publication 2004/0160237 A1 of the instant application with regards to the description of the related art within the background of the invention.

1. As per claim 1, AAPA teaches an assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to the LSI

tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

A peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation (900 figure 10 and paragraph 0003-0008);

A plurality of clock generators to generate clock asynchronous with each other and to supply the clocks to the target LSI (paragraph 0008); and

A printed circuit board (940 figure 10 and paragraph 0003).

AAPA does not specifically teach wherein on the printed circuit board the peripheral circuit and the plurality of clock generators are mounted.

However those of ordinary skill within the art at the time the invention was made would recognize that mounting the peripheral circuit and the plurality of clock generators required to generate multiple asynchronous clocks upon a printed circuit board is well known. The art is replete with references wherein electrical components/circuitry is mounted upon a printed circuit board.

Therefore those of ordinary skill within the art would be motivated to rearrange AAPA disclosing the claimed invention except for the arrangement of the peripheral circuit and plurality of clock generators mounted upon printed circuit board. It would have been obvious to one having ordinary skill within the art at the time the invention was made to mount both the peripheral circuit and plurality of clock generators upon the printed circuit board, since it has been held that rearranging parts of an invention involves only routine skill within the art. *In re Japikse,* 86 USPQ 70.

2. As per claim 12, AAPA teaches an LSI test system, comprising:

An LSI tester for supplying a test signal to a target to be tested (2 figure 10 and paragraph 0003-0008); and

An assembly for an LSI test which outputs, to the LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, wherein the assembly comprises (figure 10 and paragraphs 0003-0008),

A peripheral circuit coupled to the target LSI and allowing the target LSI to operate in the same manner as in actual operation (900 figure 10 and paragraph 0003-0008);

A plurality of clock generates to generate clock asynchronous with each other and to supply the clocks to the target LSI (paragraph 0008); and

A printed circuit board (940 figure 10 and paragraph 0003)

AAPA does not specifically teach wherein on the printed circuit board the peripheral circuit and the plurality of clock generators are mounted.

However those of ordinary skill within the art at the time the invention was made would recognize that mounting the peripheral circuit and the plurality of clock generators required to generate multiple asynchronous clocks upon a printed circuit board is well known. The art is replete with references wherein electrical components/circuitry is mounted upon a printed circuit board.

Therefore those of ordinary skill within the art would be motivated to rearrange AAPA disclosing the claimed invention except for the arrangement of the peripheral circuit and plurality of clock generators mounted upon printed circuit board. It would have been obvious to one having ordinary skill within the art at the time the invention was made to mount both the peripheral circuit and plurality of clock generators upon the printed circuit board, since it has been held that rearranging parts of an invention involves only routine skill within the art. *In re Japikse,* 86 USPQ 70.

Claims 8-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) as described within the instant application's description of the related art within the background of the invention and/or within the U.S. Publication 2004/0160237 A1 of the instant application with regards to the description of the related art within the background of the invention and in view of Fukuda (U.S. Publication 2001/0054166 A1).

3. As per claim 8, Fukuda teaches an assembly for an LSI test which supplies a test signal output from an LSI tester to a target LSI to be tested and outputs, to a LSI tester, a test result signal generated by processing of the target LSI performed in accordance with the test signal, the assembly comprising:

A test result receiving circuit for performing given processing on data obtained as the test result so as to reduce the amount of the data, and for outputting a result of the processing to the LSI tester (BIST figures 1-5 and paragraphs 0005-0007);

Fukuda does not specifically teach wherein the assembly comprises:

A plurality of clock generators to generate clock asynchronous with each other and to supply the clock to the target LSI; and

A printed circuit board on which the test result receiving circuit and the plurality of clock generators are mounted.

However AAPA teaches a plurality of clock generators to generate clock asynchronous with each other and to supply the clock to the target LSI and a printed circuit board (paragraph 0008 and figure 10 with paragraph 0003) as described above as per claims 1 and 12.

Therefore those of ordinary skill with the art at the time the invention was made would have been motivate to implement within the testing assembly as taught by Fukuda the plurality of clock generates and printed circuit board on which the test result receiving circuit and the plurality of clock generators are mounted so as to reduce the time required to fully perform the testing on an LSI.

4. As per claim 9, Fukuda teaches the assembly for an LSI test, wherein an enable control circuit for selecting necessary data from the data obtained as the test result signal and for outputting the selected data is provided in the test result receiving circuit or in the target LSI (paragraph 0007 and 0024).

5. As per claim 10, Fukuda teaches the assembly for an LSI test, wherein the test result receiving circuit includes a compression circuit for compressing input data and outputting the compressed data (paragraph 0007 and 0024).

6. As per claim 11, Fukuda as modified teaches the assembly for an LSI test as described above in detail that includes a test result receiving circuit, a plurality of clock generators, and a printed circuit board.

Fukuda as modified does not specifically teach the assembly for an LSI test, wherein the test result receiving circuit includes a determination circuit for determining whether or not the input data coincides with data to be input when the target LSI operates normally, and outputs a result of the determination.

However those of ordinary skill within the art at the time the invention was made would recognize that the test result receiving circuit (BIST) including a determination circuit for determining whether or not the input data coincides with data to be input when the target LSI operates normally, and outputs a result of the determination is well know.

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to include within the result receiving circuit (BIST) a determination circuit for determining whether or not the input data coincides with data to be input when the target LSI operates normally, and outputs a result of the determination to reduce the communications between the LSI and an external tester along with the processing time required to fully perform the testing on an LSI.

7. As per claims 14, 15, and 16, AAPA as described above in detail teaches the assembly for an LSI test comprising a peripheral circuit coupled to the target LSI, a plurality of clock generators, and a printed circuit board.

AAPA does not specifically teach the assembly for an LSI test, wherein the plurality of clock generators comprises:

A first clock generator for generators a first clock as a reference clock for the actual operation in the target LSI;

A second clock generator for generating a second clock to allow the target LSI to obtain the test signal from the LSI tester; and

A third clock generator for generating a third clock to allow the target LSI to output a test result signal.

However those of ordinary skill within the art would recognize that multiples clocks each generated by different clock generates wherein each is used to implement different operations within testing of a target LSI is well known. The art is replete with references using different clocks for different operations within testing a target LSI.

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to implement different clock generates to generate different clocks used to implement the different operations within testing of a target LSI within the AAPA assembly for testing an LSI to allow for parallel processing and/or generation of the clocks used for different operations within testing an LSI that would reduce the time required to perform the testing on an LSI.

Claims 2-4 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claim 1 above, and further in view of Ellis (U.S. Patent 6324485 B1).

8. As per claim 2, AAPA as described above in detail teaches the assembly for an LSI test comprising a peripheral circuit coupled to the target LSI, a plurality of clock generators, and a printed circuit board.

AAPA does not specifically teach wherein the assembly for an LSI test includes:

A first board including the peripheral circuit and the printed circuit board; and

A second board coupled to the first board and including wiring for coupling the first board and the LSI tester to each other.

However in an analogous art Ellis teaches of a LSI test assembly including a first board including circuitry disposed upon it for testing, and a second board coupled to the first board and including wiring for coupling the first board and an LSI tester to each other (see figures 1A, 2, 3 and column 1 lines 28-41 and column 5 line 57 – column 6 line 5).

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to incorporate Elli's first and second boards within AAPA LSI testing assembly so as to easily interface a target LSI desired to be tested with the system or circuitry desired to test the target LSI.

9. As per claim 3, AAPA teaches wherein the test signal is supplied to the peripheral circuit and then output from the peripheral circuit to the target LSI (figure 10 and paragraphs 0005 and 0008).

10. As per claim 4, AAPA teaches wherein the test result signal is supplied to the peripheral circuit and then output from the peripheral circuit to the LSI tester (figure 10 and paragraphs 0005 and 0008).

Claims 5-7 are rejected under 35 U.S.C. 103(a) as being unpatentable over AAPA as applied to claim 1 above, and further in view of Fukuda (U.S. Publication 2001/0054166 A1).

11. As per claim 5, AAPA as described above in detail teaches the assembly for an LSI test comprising a peripheral circuit coupled to the target LSI, a plurality of clock generators, and a printed circuit board.

AAPA does not specifically teach the assembly for an LSI test, wherein a memory is provided as the peripheral circuit or in the target LSI, and the LSI tester is configured to be capable of accessing the memory asynchronously to a clock supplied to the target LSI.

However in an analogous art Fukuda teaches of a built-in self-test (BIST) that is accessible by a tester asynchronously to a clock supplied to the LSI being tested wherein the BIST acts as a memory (figures 1-5 and paragraphs 0002-0007).

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to incorporate the BIST memory accessible by a test asynchronously to a clock supplied to the LSI being tested wherein the BIST acts as a memory as taught by Fukuda within AAPA assembly for testing a LSI with the BIST memory provided as the peripheral circuit or in the target LSI to easily access and test hard to access circuit within a target LSI and reduce timely communications between an external tester and the target LSI being tested.

12. As per claim 6, Fukuda teaches the assembly for an LSI test, wherein the test signal is stored in the memory, and then read out from the memory to be processed by the target LSI (figures 1-5 and paragraphs 0005-0007 and 0024).

13. As per claim 7, Fukuda teaches the assembly for an LSI test, wherein the test result signal is stored in the memory, and then read out from the memory to the LSI tester (figures 1-5 and paragraph 0005).

Claim 13 is rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant Admitted Prior Art (AAPA) as described within the instant application's description of the related art within the background of the invention and/or within the U.S. Publication 2004/0160237 A1 of the instant application with regards to the description of the related art within the background of the invention as modified as per claim 14 and 16 or in further view of Fukuda (U.S. Publication 2001/0054166 A1) as modified with AAPA as per claim 15.

14. As per claim 13, AAPA as modified or Fukuda as modified with AAPA as described above as per claims 14-16 teaches the LSI testing assembly of testing an LSI with a plurality of clocks and/or signals.

AAPA as modified or Fukuda as modified with AAPA does not specifically teach wherein the assembly is executed with an LSI test method, comprising the steps of:

> Operating a non-defective LSI, which is configured as a target LSI to be tested and has been confirmed to operate normally, in a circuit equivilate to a circuit actually used, and generating and storing a test signal and a reference test result signal, based on a signal supplied to the non-defective LSI and a signal

output from the non-defective LSI, respectively, wherein the circuit comprises a plurality of clock generators to generate clocks asynchronous with each other and to supply the clocks to the target LSI, and

Supply the test signal to the target LSI synchronized with a first one of the clocks;

Carrying out the actual operation for the target LSI synchronized with a second one of the clocks;

Outputting the test result signal from the target LSI synchronized with a third one of the clocks; and

Determining whether or not the target LSI is defective by comparing the test result signal with reference test result signal.

However those of ordinary skill within the art at the time the invention was made would recognize that retesting an LSI that has already been confirmed to operate normally is well know, as are the steps and clocks used in retesting an LSI. The art is replete with references wherein a device under test (DUT) such as an LSI is retested.

Therefore those of ordinary skill within the art at the time the invention was made would have been motivated to incorporate retesting of a confirmed to operate normally and thus non-defective LSI within the assembly/method of AAPA with or without being modified with Fukuda and/or Ellis to ensure that the confirmed non-defective operating normally LSI is truly non-defective and operating within the normal parameters with which the LSI is to operate within, and that no errors were introduced into the LSI as a result of the testing performed up on the LSI.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

i. Ellis (U.S. Patent 6324485 B1) discloses known good DUT being tested or retested within a test system (see specifically column 9 lines 31-34).

ii. Distler et al (U.S. Publication 2002/0099992 A1) discloses data compression within a product under test (PUT) or within a tester to reduce the size of the date to only the data needed for comparison. (paragraph 0009)

iii. Johnson (U.S. Patent 5416784) discloses a number of clocks, specifically a normal clock, test clock, and output clock.

iv. Ooishi (U.S. patent 6421789 B1) discloses a clock generating circuit for generating an operation clock along with a test clock generation circuit in addition to output clocks.

v. Lloyd et al (U.S. Patent 3733587) discloses retesting a unit under test (UUT).

vi. JP 07-128405 (provided by applicant within the IDS filed in the office on 08/11/2003) discloses a vertical three-step structure that allows a device to be applied to any kind of device to be tested having different arrangement of pins or different number of pins. Noted that pins are the

connection pints at the beginning and/or end of wiring paths within/on a structure.

vii. JP 04-155278 (provided by applicant within the IDS filed in the office on 07/07/2004) discloses a memory circuit for storing test patterns within an LSI (see abstract).

viii. WO 02/29824 (provided by applicant within the IDS filed in the office on 07/07/2004) discloses a references device being tested and comparing the reference device to a DUT (claim 1).

ix. "Major Problems and Solutions of the System LSI testing" (provided by applicant within the IDS filed in the office on 08/11/2003) discloses BIST (Built-In Self Test), SCAN testing, and data compression.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Steven D. Radosevich whose telephone number is 571-272-2745. The examiner can normally be reached on 9am-5:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 571-272-3819. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Steven D. Radosevich
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